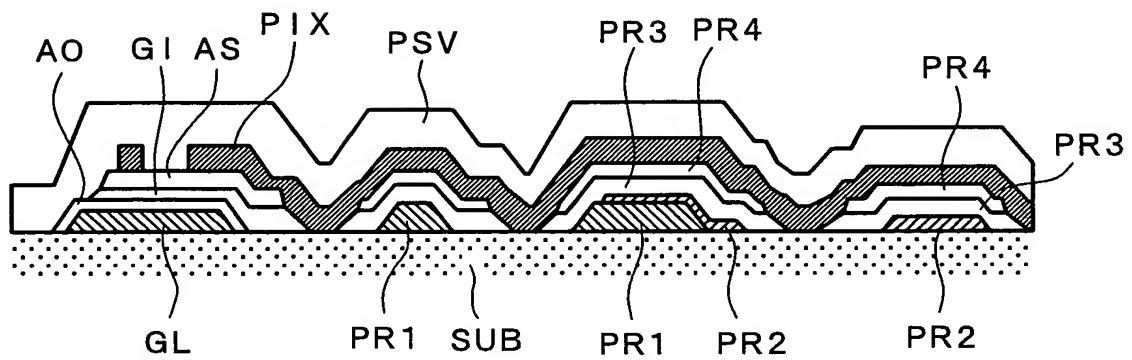
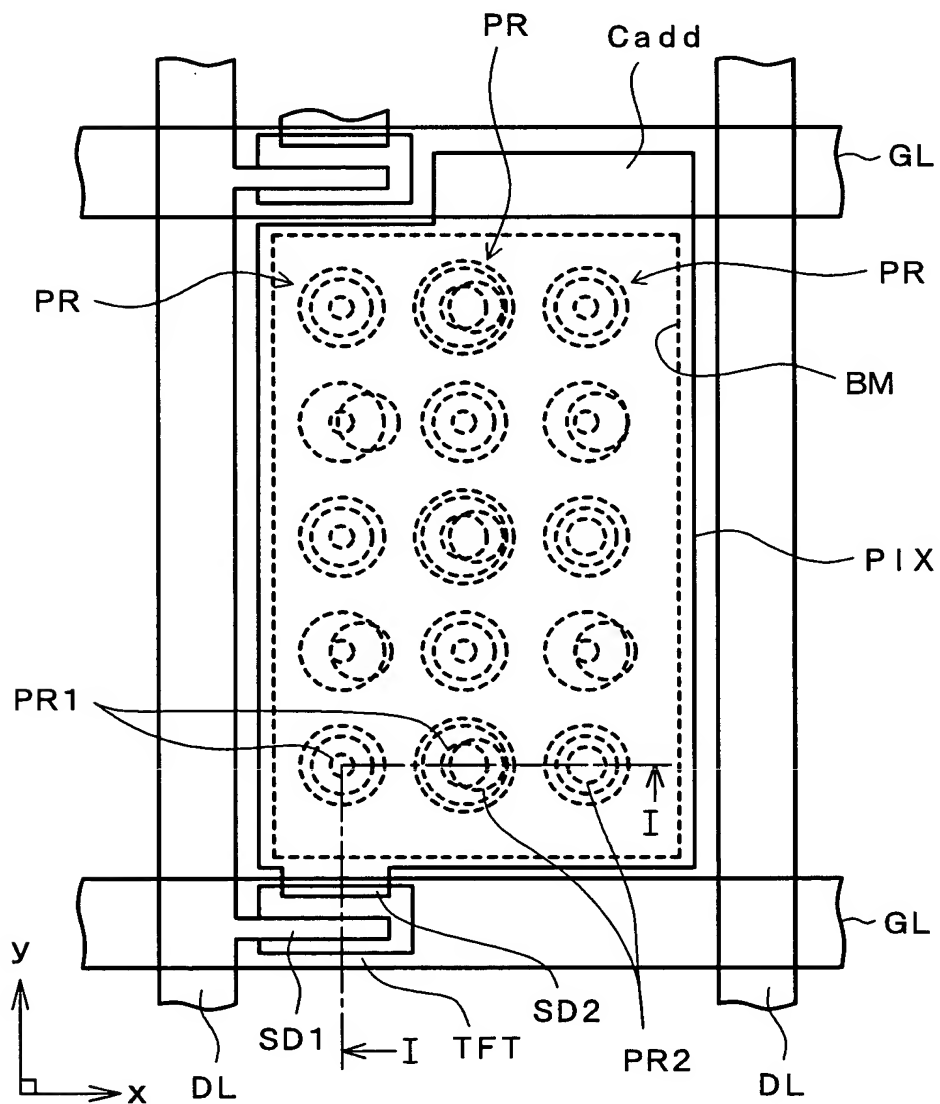


*FIG. 1*



*FIG. 2*

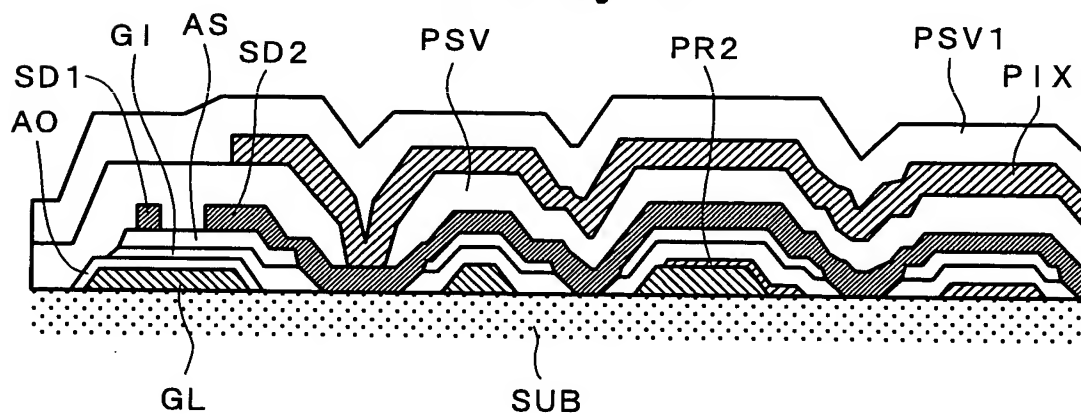


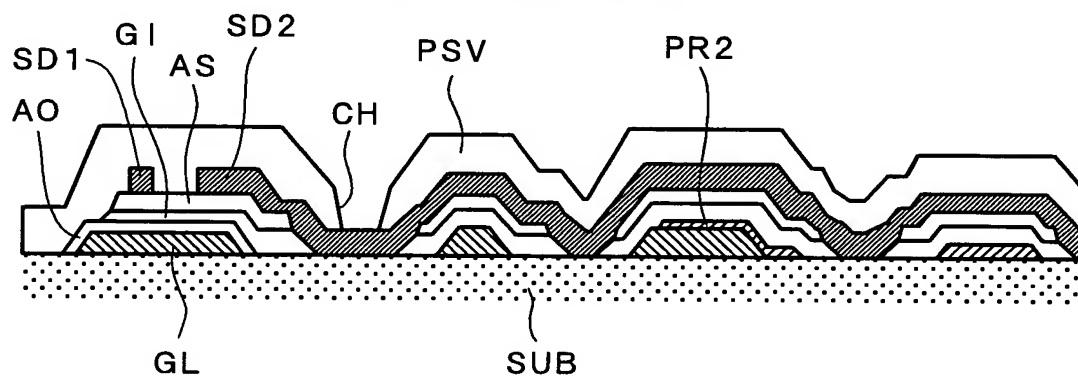
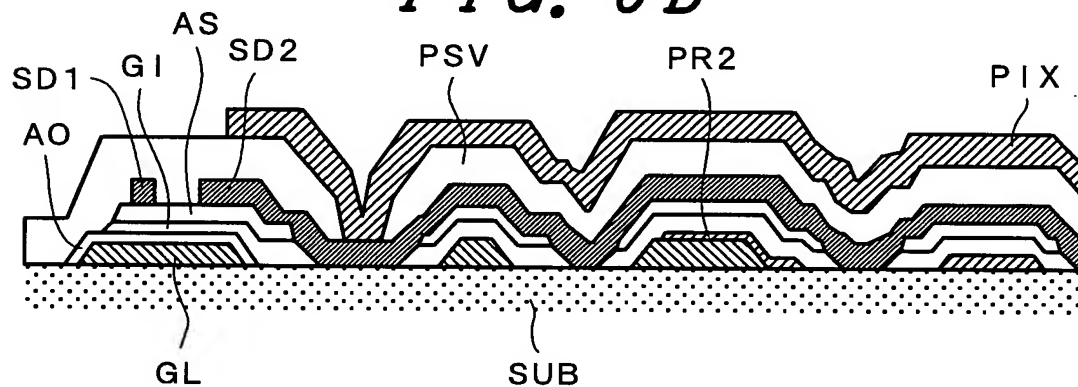
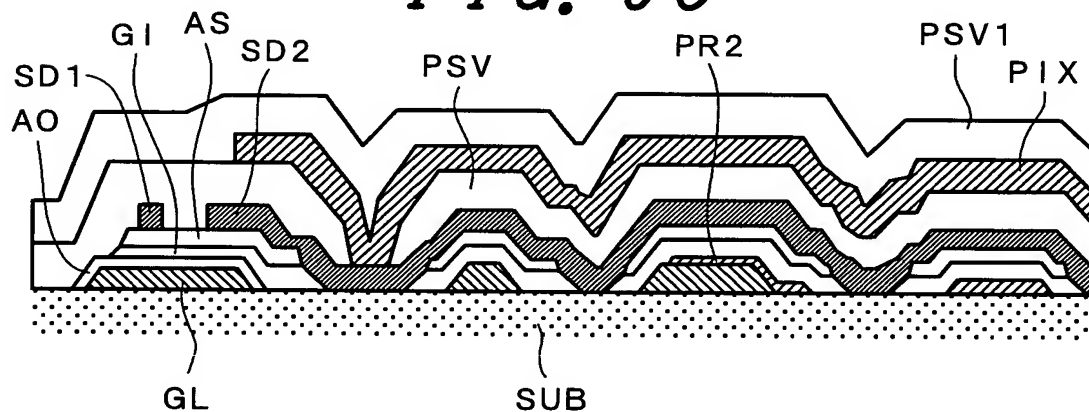
A cross-sectional view of a semiconductor device. It shows a substrate (SUB) with a gate layer (GL) and two pass regions (PR1). The gate layer (GL) is a thin layer on the substrate. The pass regions (PR1) are regions where the gate layer is not present, allowing for electrical contact or other functions.

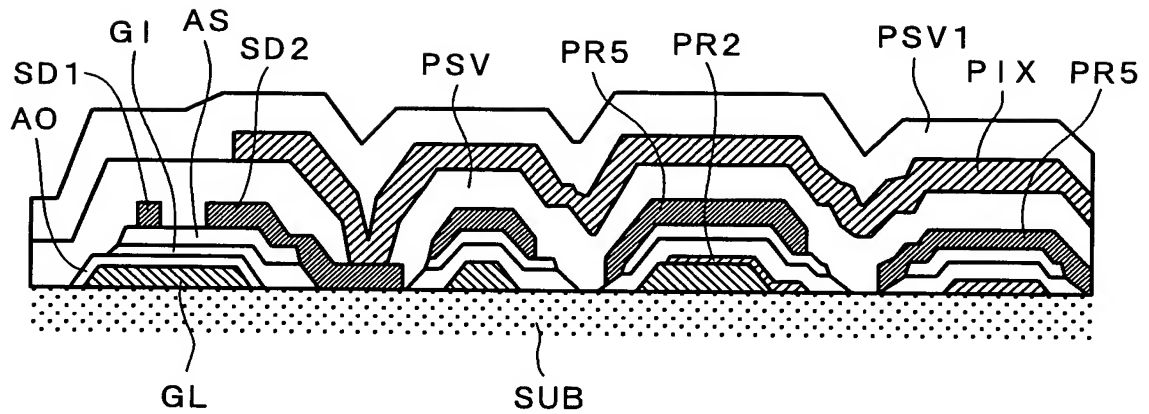
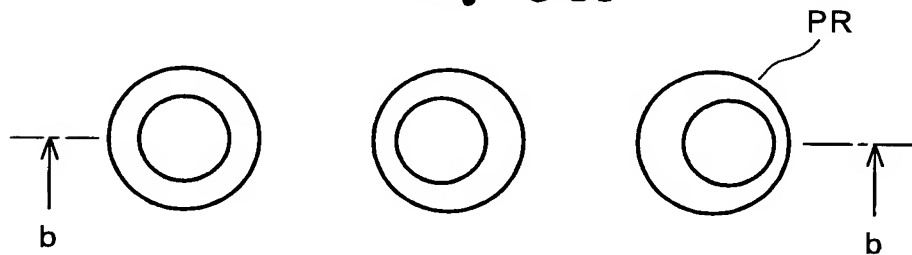
A cross-sectional view of a semiconductor device. A substrate (SUB) is shown with a gate layer (GL) on top. A passivation layer (AO) is deposited over the gate layer. Two pairs of contact pads are formed: the first pair is labeled PR1 and the second pair is labeled PR2. The pads are made of a conductive material, indicated by hatching.

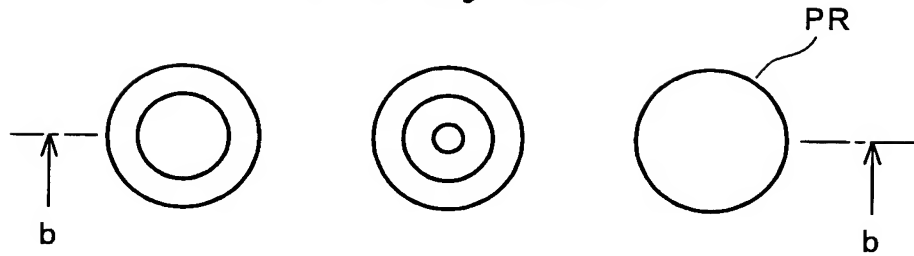
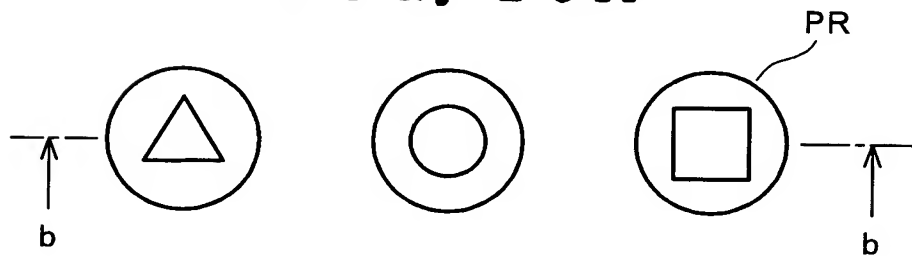
A cross-sectional diagram of a semiconductor device structure. The diagram shows a substrate (SUB) with a dotted pattern. On top of the substrate is a layer labeled GL (gate layer) with a diagonal hatching pattern. Above the GL layer is a complex structure consisting of several layers: a bottom layer with diagonal hatching, a layer with a wavy pattern labeled PIX, a layer with a solid white pattern labeled PSV, and a top layer with a solid white pattern labeled AS. A label AO points to the left side of the structure. The structure is composed of repeating rectangular blocks separated by recessed areas.

[illegible]

[illegible]

*FIG. 6A**FIG. 6B**FIG. 6C*

*FIG. 7**FIG. 8A**FIG. 8B*

*FIG. 9A**FIG. 9B**FIG. 10A**FIG. 10B*

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